REMARKS

This Amendment responds to the Office Action dated October 6, 2009, in which the Examiner rejected claims 1-19 under 35 U.S.C. § 103.

As indicated above, claims 1 and 5 have been amended in order to make explicit what is implicit in the claims. The amendment is unrelated to a statutory requirement for patentability. Claims 3-4, 7-8 and 17-19 have been amended to correspond to the amendments made to claims 1 and 5. The amendments are unrelated to a statutory requirement for patentability and do not narrow the literal scope of the claims.

Claims 1 and 5 claim an image pick-up device comprising a pick-up means/portion, control means/portion, frame-addition processing means/portion, a frame rate conversion means/portion and a monitor image generation means/portion. The control means/portion generates a synchronization signal. The image signal pick-up means/portion is connected to the control means/portion and picks up an image signal with a varied frame-rate. The frame-addition processing means/portion is connected to the image signal pick-up means/portion and the control means/portion. The frame-addition processing means/portion generates a first image signal from the variable frame-rate picked-up image signal, with a selected output frame rate based upon the synchronization signal. The frame rate conversion mean/portion is connected to the control means/portion and an external device. The frame rate conversion means/portion converts a frame rate of a second image signal, supplied from the external device, to the output frame rate of the first image signal based upon the synchronization signal. The monitor image generation means/portion is connected to the frame-addition processing means/portion and the frame rate conversion means/portion. The monitor image generation means/portion generates a

monitor image signal for display by a monitor by using the first image signal and the second image signal.

By (a) generating a synchronization signal via a control means/portion, (b) generating a first image signal with a selected output frame rate based upon the synchronization signal, (c) converting the frame rate of a second image signal supplied from an external device to the output frame rate of the first image signal based upon the (same) synchronization signal and (d) interconnecting the control means/portion, frame-addition processing means/portion, frame rate conversion means/portion and monitor image generation means/portion as claimed in claims 1 and 5, the claimed invention provides an image-pick-up device that can accept an external input video signal whose frame rate is different from the output frame rate of the pick-up device in order to monitor a picked-up image as well as a reproduced image which can be simultaneously displayed on one screen even though the images have different frame rates. The prior art does not show, teach or suggest the invention as claimed in claims 1 and 5.

Claims 1-19 were rejected under 35 U.S.C. § 103 as being unpatentable over *Asada, et al.* (U.S. Publication No. 2002/0021364), *Tonomura* (JP 11-177930), *Weisgerber* (U.S. Patent No. 5,739,894) and *Chen, et al.* (U.S. Patent No. 5,453,780).

Asada, et al. appears to disclose in Figure 8 a charge coupled device (CCD) 1 operable for a progressive scanning, a CCD driver 2, a drive pulse switching circuit 3 for selecting and issuing a CCD drive pulse corresponding to a multi-frame rate, a frame memory 40, a camera signal processing circuit 5 for performing a camera process, a view finder (VF) 6 operable in a progressive scanning, a VCR unit 24 for recording and reproducing a multi-frame rate signal and a reproduced signal convertor 25 for converting the frame rate of a reproduced signal [0055].

Thus, *Asada, et al.* merely discloses a CCD 1, driver 2, switching circuit 3, camera signal processing circuit 5, view finder 6, VCR unit 24 and reproduced signal convertor 25. Nothing in *Asada, et al.* shows, teaches or suggests (a) a control means/portion generating a synchronization signal, (b) a frame-addition processing means/portion generating a first signal with a selected output frame rate based upon the synchronization signal, (c) a frame-rate conversion means/portion converting a frame rate of a second image signal supplied from an external device to the output frame rate of the first image signal based upon the (same) synchronization signal and (d) monitor image generation means/portion generating a monitor image signal for display by a monitor using the first and second image signals as claimed in claims 1 and 5. Rather, *Asada, et al.* only discloses CCD 1, driver 2, switching circuit 3, camera signal processing circuit 5, view finder 6 and VCR unit 24.

Furthermore, *Asada, et al.* merely discloses in Figure 8 a camera signal processing circuit 5 connected to the view finder 6, frame memory 4 and VCR unit 24. Nothing in *Asada, et al.* shows, teaches or suggests (a) a control means/portion connected to an image signal pick-up means/portion, frame-addition processing means/portion and frame rate conversion means/portion, (b) the frame-addition processing means/portion connected to the image signal pick-up means and monitor image generation means/portion and (c) a frame rate conversion means/portion additionally connected to an external device and the monitor image generation means/portion as claimed in claims 1 and 5. Rather, *Asada, et al.* only discloses a camera signal processing circuit 5 connected to a frame memory 4, view finder 6 and VCR unit 24.

Tonomura appears to disclose reading out a picture signal from an image sensor [0009]. The picture signal generated by the photo electric conversion in the CCD imager 1 is sent to a

processor 2 for predetermined video processing. The picture signal from the processor circuit 2 is sent to and recorded by the recording reproduction section 3. If driving timing of the CCD imager 1 and writing timing of the picture signal in the recording reproduction section 3 are made into arbitrary frame rates 3X or less, recording timing circuit 5 will manage them [0013]. A reference synchronizing signal supplied by a terminal 9 is input into reproduction timing circuit 6. The synchronization with the reference synchronizing signal, the reproduction timing managed by the reproduction timing circuit 6 is reproduced by a 1X frame rate and the picture signal currently recorded on the recording reproduction section 3 is sent to a processor circuit 4. The processor circuit 4 performs predetermined signal processing to the picture signal supplied from the recording reproduction section 3 and outputs the signal to a video output terminal 8 [0014].

Thus, *Tonomura* merely discloses that when recording a signal from processor 2 having one frame rate to the recording/reproducing apparatus 3 at a different frame rate, a recording timing circuit 5 manages the signals. Thus, nothing in *Tonomura* shows, teaches or suggests (a) a control means/portion generating a synchronization signal, (b) a frame-addition processing means/portion generating a first image signal with a selected output frame rate based upon the synchronization signal, (c) a frame rate conversion means/portion converting the frame rate of a second image signal supplied from an external device to the output frame rate of the first image signal based upon the (same) synchronization signal, and (d) monitor image generation means/portion generating a monitor image signal for display by a monitor using the first and second image signals as claimed in claims 1 and 5. Rather, *Tonomura* only discloses a recording timing circuit 5 managing the difference between the driving timing of the CCD imager 1 and the writing timing of the picture signal in the recording reproduction section 3.

Additionally, *Tonomura* merely discloses a recording/reproducing circuit 3 connected to a processor 2, recording timing circuit 5, reproduction timing circuit 6 and processor 4. Nothing in *Tonomura* shows, teaches or suggests the interconnection of the circuits as claimed in claims 1 and 5 (*i.e.* an image signal pick-up means/portion connected to a control means/portion, a frame-addition processing means/portion connected to the image signal pick-up means/portion and control means/portion, the frame rate conversion means/portion connected to the control means/portion and an external device and a monitor image generation means/portion connected to the frame-addition processing means/portion and frame rate conversion means/portion) as claimed in claims 1 and 5. Rather, *Tonomura* only discloses a record/reproduction device 3 connected to a recording timing circuit 5, reproduction timing circuit 6 and processors 2, 4.

Weisgerber appears to disclose presentation of motion pictures with audience impact by compositing separate image components onto a strip of film with some components having a "cinematic" look and other components having a highly realistic look. This is done by using two different frame rates to photograph the scenes or image components and projecting the film in question at the higher of the frame rates (column 3, lines 10-17). Certain image components are photographed or printed at a frame rate of 30 frames per second or less. By contrast, other image components are photographed or printed at a frame rate in excess of 30 frames per second. These two sequences photographed at different rates are composited or cut together onto a single strip of film to produce an image that appears highly realistic in part and "cinematic" in the other (column 4, lines 48-67). Figure 4 of *Weisgerber* merely discloses recording film images onto separate film strips at two different frame rates, compositing these image components onto another film strip and this film strip is then projected at the higher of the two frame rates (column 4, lines 35-43).

Thus, *Weisgerber* only discloses a method of compositing separate film strips onto another film strip. Nothing in *Weisgerber* shows, teaches or suggests (a) control means/portion generating a synchronization signal, (b) frame rate conversion means/portion converting a frame rate of a second image signal supplied from an external device, to the output frame rate of the first image signal based upon the (same) synchronization signal, (c) a frame-addition processing means/portion generating a first image signal with a selected output frame rate based upon a synchronization signal and (d) a monitor image generation means/portion generating a monitor image signal for display by a monitor using the first and second image signals as claimed in claims 1 and 5. Rather, *Weisgerber* only discloses a projector which projects a film strip of composited film strips.

Furthermore, *Weisgerber* only discloses in Figure 4 film images recorded onto separate film strips at two different frame rates are then composited onto another film strip which is projected at the higher of the two frame rates. Nothing in *Weisgerber* shows, teaches or suggests the interconnection of the various means as claimed in claims 1 and 5 (*i.e.* an image signal pick-up means/portion connected to a control means/portion, frame-addition processing means/portion connected to an image signal pick-up means/portion and control means/portion, frame rate conversion means/portion connected to the control means/portion and external device and monitor image generation means/portion connected to the frame-addition processing means/portion and frame rate conversion means/portion). Rather, *Weisgerber* only discloses recording film images onto two different film strips and then compositing the two components onto another film strip.

Chen, et al. appears to disclose a remote classroom application in Figure 6 where MCU 601 combines 4 QCIF digital video signals of four students 602-605 from four classrooms sites that are remote from the site of the teacher 606. The MCU 601 combines the 4 QCIF input video signals, each at rate R into a CIF digital video signal, at rate 4R that is transmitted to the teacher's terminal 607. The teacher can thus see each of the four students simultaneously (col. 4, lines 44-51). Figure 7 shows that architecture of the MCU or video signal combiner 700. Four digital input streams from four multiparty video conference participants are input on lead 701-704 to network interface circuit 705 (column 4, lines 58-63). Network interface circuitry 705 polls the frame rate of each of the terminals to determine the lowest common frame-rate capability of the terminals. The syntax is then peeled-off each input signal and input to an associated buffer 706-709. Input to each buffer 706-709 is therefore a data stream that consists of sequential digital video frames transmitted by the corresponding conference participants terminal (column 5, lines 2-12). Each of the buffers 706-709 is connected to a combiner processor 710 which performs the functions of data parsing, frame synchronization, buffer management and data formatting for output to multiplexor 711 (column 5, lines 22-25). Processor 710 retrieves from buffer 706-709 the GOBs which multiplexer 711 combines in a time-division multiplexed manner to form the combined CIF signal (column 5, lines 41-44). Multiplexer 711 outputs a single CIF digital video signal comprising the combined and regrouped GOBs (column 5, lines 61-63).

Thus, *Chen, et al.* merely discloses a processor 710 which performs the function of data parsing, frame synchronization, buffer management and data formatting for output to a multiplexer 711. Nothing in *Chen, et al.* shows, teaches or suggests (a) control means/portion generating a synchronization signal, (b) frame-addition processing means/portion generating a first image signal with a selected output frame rate based upon the synchronization signal, (c) a

frame rate conversion means/portion converting the frame rate of a second image signal to the output frame rate of the first image signal based upon the synchronization signal and (d) monitor image generation means/portion generating a monitor image signal for display by a monitor using the first and second image signals as claimed in claims 1 and 5. Rather, *Chen, et al.* only discloses a combiner processor 710 that performs frame synchronization.

Additionally, *Chen, et al.* merely discloses in Figure 7 a combiner processor 710 connected to buffer 706-709 and multiplexer 711. Thus, nothing in *Chen, et al.* shows, teaches or suggests (a) an image signal pick-up means connected to a control means/portion, (b) a frame-addition processing means/portion connected to an image signal pick-up means/portion and control means/portion, (c) frame rate conversion means/portion connected to the control means/portion and an external device and (d) a monitor image generation means/portion connected to the frame-addition processing means/portion and frame-rate conversion means/portion as claimed in claims 1 and 5. Rather, *Chen, et al.* only discloses a combiner processor 710 connected to buffers 706-709 and multiplexor 711.

A combination of *Asada, et al.*, *Tonomura*, *Weisgerber* and *Chen, et al.* would merely suggest that after outputting the signals from CCD 1 of *Asada, et al.* to control the writing of the signals to a reproduction device by a recording circuit as taught by *Tonomura*, to record the images onto film strips which are then composited into a single film as taught by *Weisgerber* and to have a combiner processor perform frame synchronization between buffers and a multiplexer as taught by *Chen, et al.* Thus, nothing in the combination of the references shows, teaches or suggests (a) control means/portion generating a synchronization signal, (b) frame-addition processing means/portion generating a first image signal with a selected output frame rate based

upon the synchronization signal, (c) a frame rate conversion means/portion converting a frame rate of a second image signal supplied from an external device to the output frame rate of the first image signal based upon the same synchronization signal, (d) a monitor image generation means/portion generating a monitor image signal for display by a monitor using the first and second image signals and (e) interconnecting the control means/portion, image signal pick-up means/portion, frame-addition processing means/portion, frame rate conversion means/portion and monitor image generation means/portion as claimed in claims 1 and 5. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 1 and 5 under 35 U.S.C. § 103.

Claims 2-4, 6-14 and 17-19 recite additional features. Applicants respectfully submit that claims 2-4, 6-14 and 17-19 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Asada, et al.*, *Tonomura*, *Weisgerber* and *Chen, et al.* at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 2-4, 6-14 and 17-19 under 35 U.S.C. § 103.

Thus it now appears that the application is in condition for a reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

CONCLUSION

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 50-0320.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 50-0320.

Respectfully submitted,

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